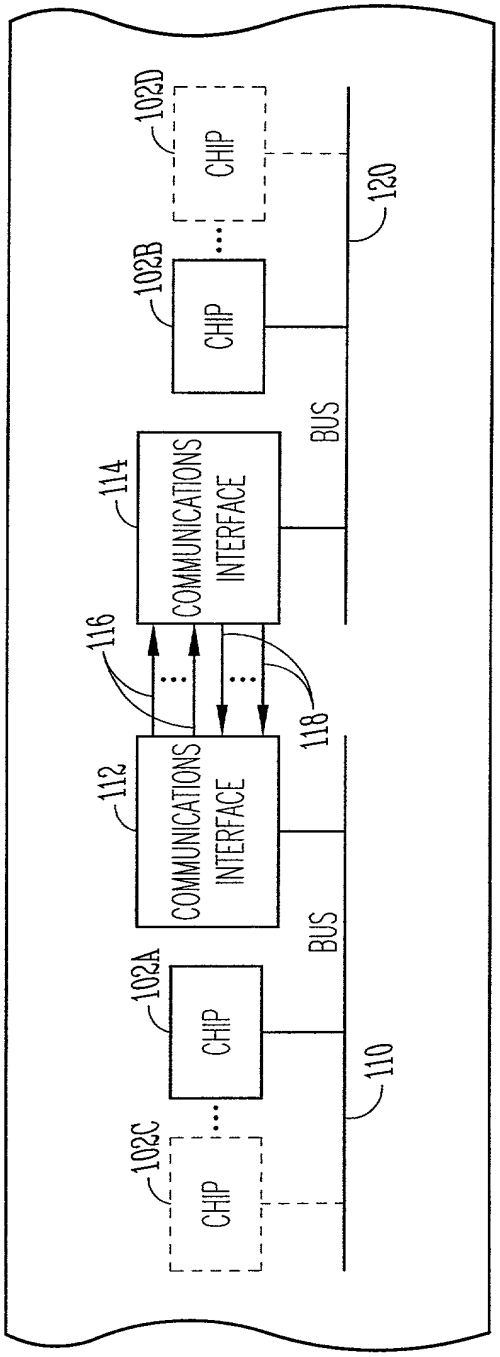
102D
CHIP
120
102B
CHIP
BUS
114
COMMUNICATIONS INTERFACE
116
118
112
COMMUNICATIONS INTERFACE
BUS
102A
CHIP
110
102C
CHIP

Fig.1

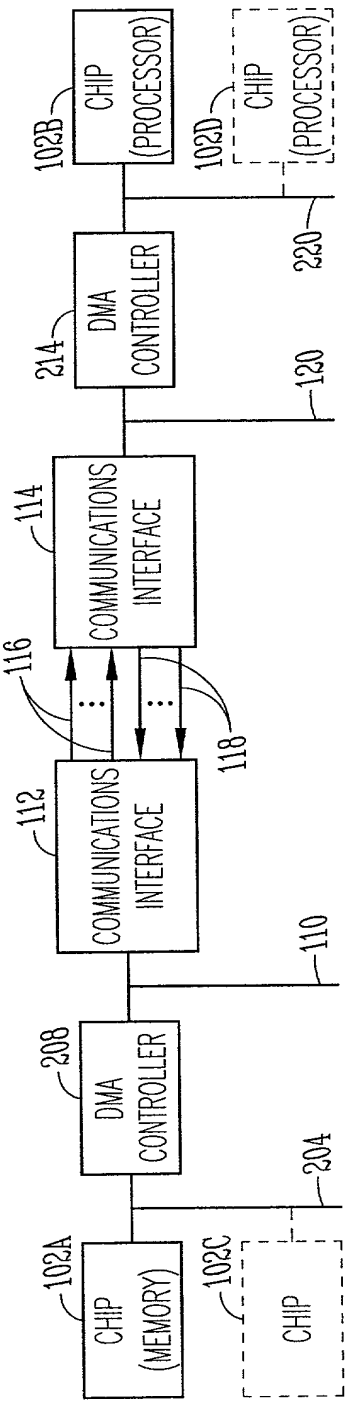
102A
CHIP (MEMORY)
102C
CHIP
102B
CHIP (PROCESSOR)
102D
CHIP (PROCESSOR)
208
DMA CONTROLLER
214
DMA CONTROLLER
112
COMMUNICATIONS INTERFACE
114
COMMUNICATIONS INTERFACE
116
118
110
120
204
220

Fig.2

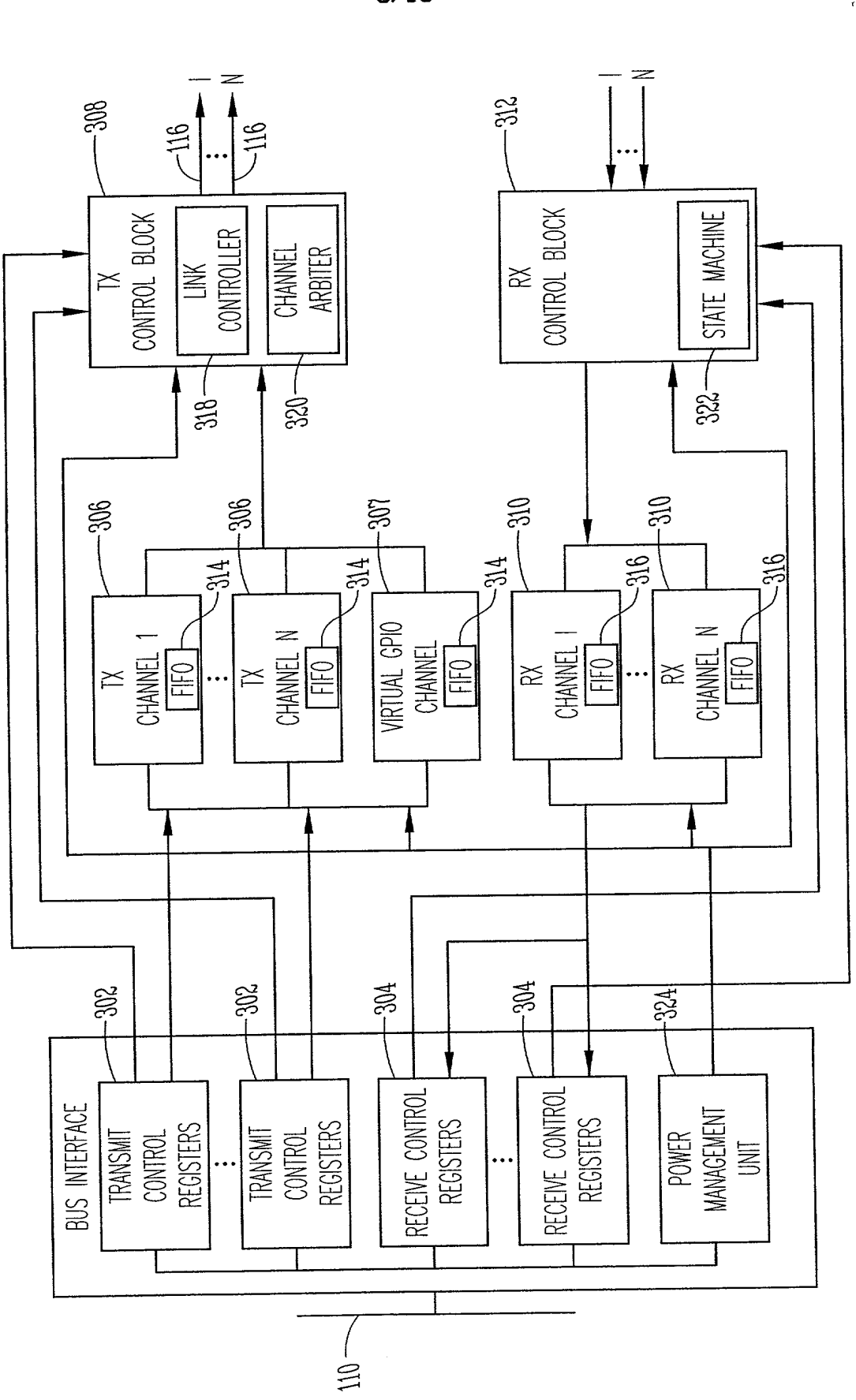
112
308
116
1
N
116
TX CONTROL BLOCK
LINK CONTROLLER
CHANNEL ARBITER
318
320
312
RX CONTROL BLOCK
STATE MACHINE
322
306
306
307
310
310
314
314
314
316
316
TX CHANNEL 1
FIFO
TX CHANNEL N
FIFO
VIRTUAL GPIO CHANNEL
FIFO
RX CHANNEL 1
FIFO
RX CHANNEL N
FIFO
302
302
304
304
324
BUS INTERFACE
TRANSMIT CONTROL REGISTERS
TRANSMIT CONTROL REGISTERS
RECEIVE CONTROL REGISTERS
RECEIVE CONTROL REGISTERS
POWER MANAGEMENT UNIT
110

Fig.3

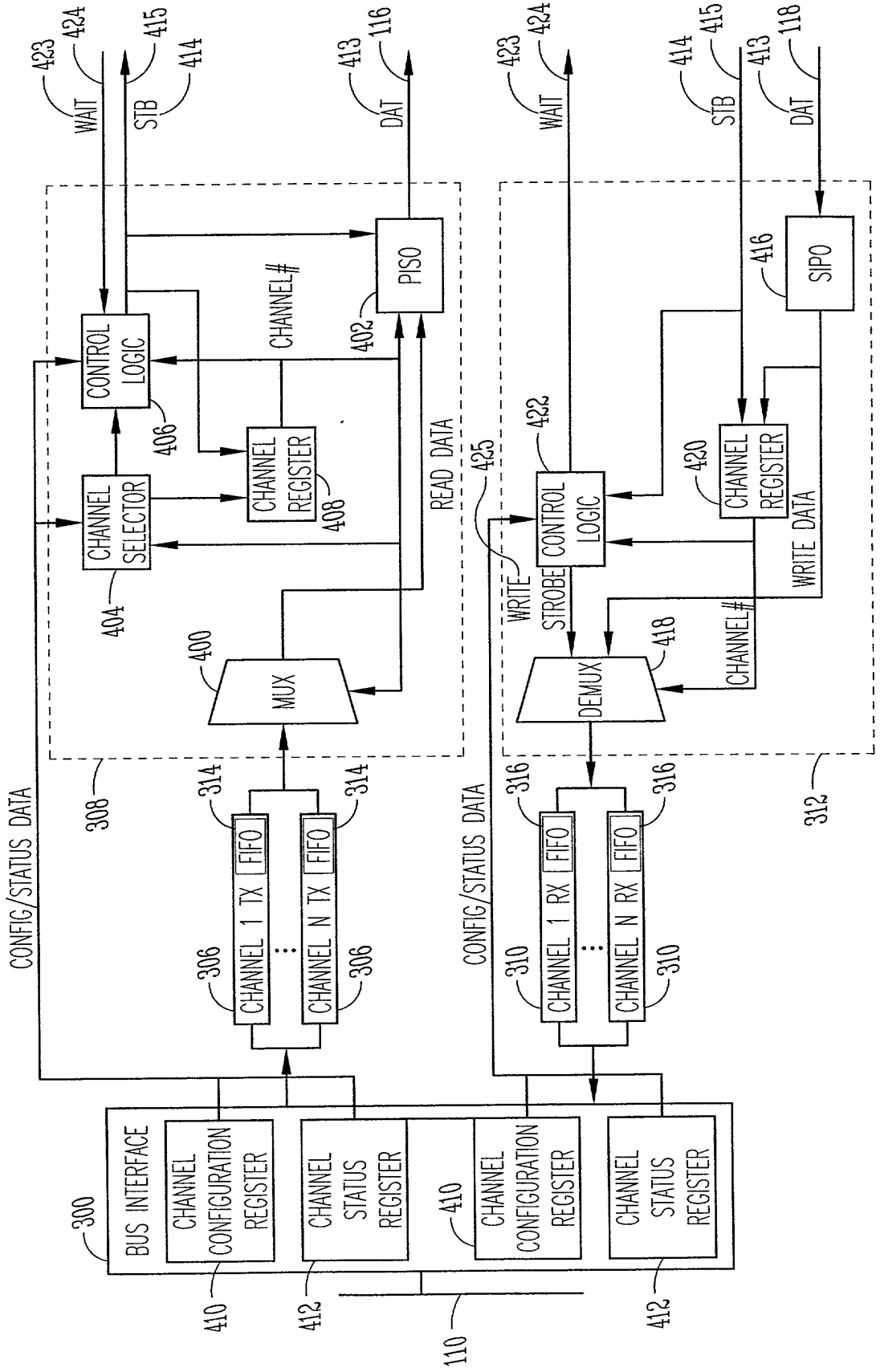
112
423
424
WAIT
415
STB
414
413
116
DAT
CONTROL LOGIC
406
CHANNEL#
PISO
402
CHANNEL SELECTOR
404
CHANNEL REGISTER
408
READ DATA
400
MUX
308
314
CHANNEL 1 TX
FIFO
CHANNEL N TX
306
CONFIG/STATUS DATA
BUS INTERFACE
300
CHANNEL CONFIGURATION REGISTER
410
CHANNEL STATUS REGISTER
412
110
423
424
WAIT
422
425
WRITE
STROBE
CONTROL LOGIC
DEMUX
418
CHANNEL#
414
415
STB
413
118
DAT
416
SIPO
420
CHANNEL REGISTER
WRITE DATA
312
316
CHANNEL 1 RX
CHANNEL N RX
310
CONFIG/STATUS DATA
410
CHANNEL CONFIGURATION REGISTER
412
CHANNEL STATUS REGISTER

Fig.4

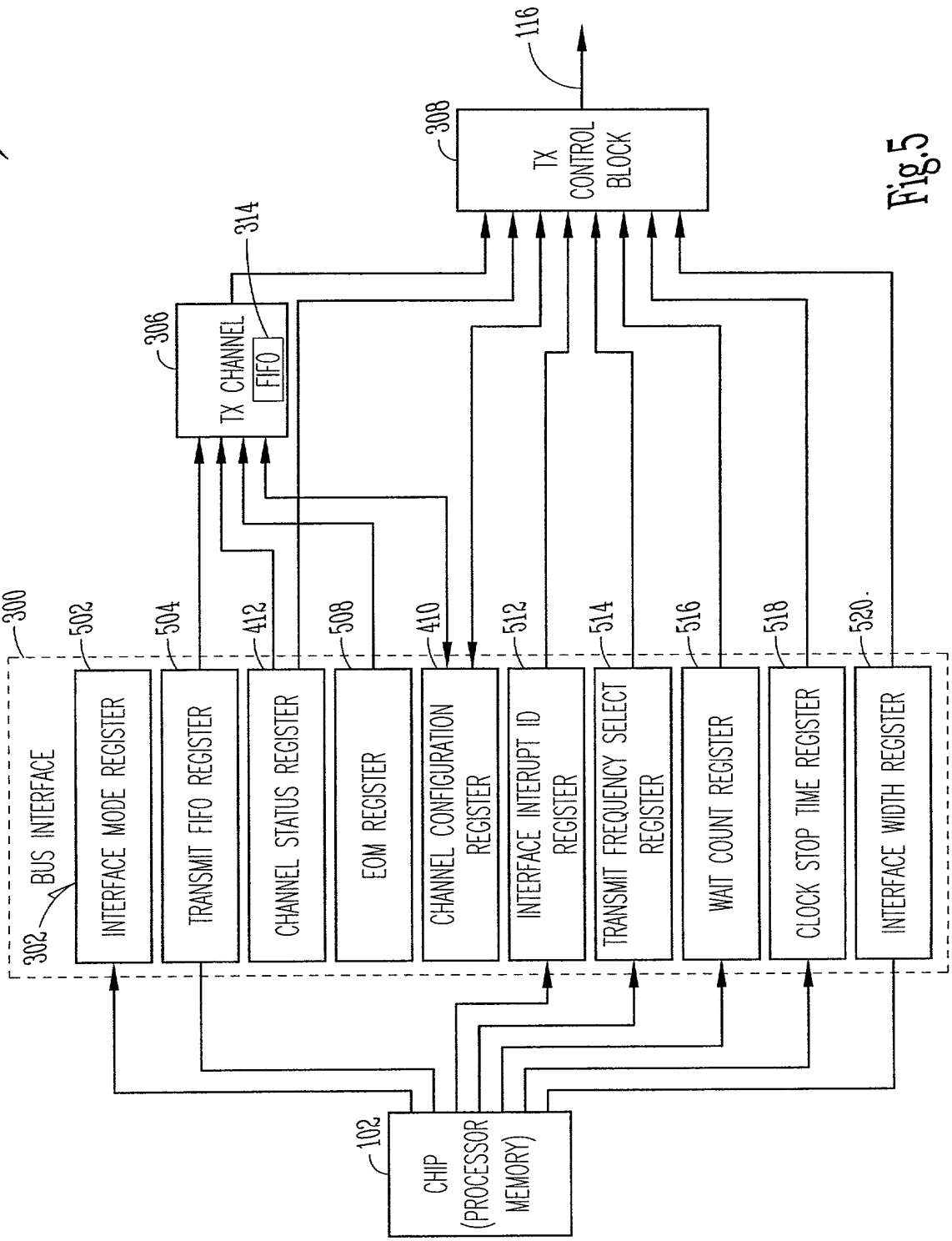
112
116
308
TX CONTROL BLOCK
314
306
TX CHANNEL
FIFO
300
BUS INTERFACE
302
502
504
412
508
410
512
514
516
518
520
INTERFACE MODE REGISTER
TRANSMIT FIFO REGISTER
CHANNEL STATUS REGISTER
EOM REGISTER
CHANNEL CONFIGURATION REGISTER
INTERFACE INTERUPT ID REGISTER
TRANSMIT FREQUENCY SELECT REGISTER
WAIT COUNT REGISTER
CLOCK STOP TIME REGISTER
INTERFACE WIDTH REGISTER
102
CHIP (PROCESSOR MEMORY)

Fig.5

412

	CHANNEL STATUS REGISTER BIT LAYOUT AND DEFINITIONS			
	BITS	ACCESS	NAME	DESCRIPTION
	31:26	N/A	RESERVED	RESERVED
602	25	READ	RxEOM	RECEIVE CHANNEL RECIEVED EOM • 0=CHANNEL DID NOT RECIEVE EOM • 1=CHANNEL RECIEVED EOM
604	24	READ	RxWAIT	RECEIVE CHANNEL IN WAIT STATE • 0=CHANNEL NOT IN WAIT STATE • 1=CHANNEL IN WAIT STATE
606	23	READ	RxEMPTY	RECEIVE FIFO EMPTY • 0=NOT EMPTY • 1=EMPTY
608	22	READ	RxFULL	RECEIVE FIFO FULL • 0=NOT FULL • 1=FULL
610	21:16	READ	RxFULLNESS	FULLNESS OF RECEIVE FIFO • 000000=FIFO IS EITHER FULL OR EMPTY (SEE RxFULL AND RxEMPTY BITS) • NONZERO=NUMBER OF BYTES OF DATA IN RECEIVE FIFO
	15:9	N/A	RESERVED	RESERVED
604	8	READ	TxWAIT	TRANSMIT CHANNEL IN WAIT STATE • 0=CHANNEL NOT IN WAIT STATE • 1=CHANNEL IN WAIT STATE
606	7	READ	TxEMPTY	TRANSMIT FIFO EMPTY • 0=NOT EMPTY • 1=EMPTY
608	6	READ	TxFULL	TRANSMIT FIFO FULL • 0=NOT FULL • 1=FULL
610	5:0	READ	TxFULLNESS	FULLNESS OF TRANSMIT FIFO • 000000=FIFO IS EITHER FULL OR EMPTY (SEE TxFULL AND TxEMPTY BITS) • NONZERO=NUMBER OF BYTES OF DATA IN TRANSMIT FIFO

Fig.6

412

CHANNEL CONFIGURATION REGISTER BIT LAYOUT AND DEFINITIONS			
BITS	ACCESS	NAME	DESCRIPTION
31:26	N/A	RESERVED	RESERVED
25:24 (702)	READ/WRITE	EOCSERVICE	EARLY EOC SERVICE SELECT • 00=NONE • 01=INTERRUPT • 1x=RESERVED
23:21 (704)	READ/WRITE	RxSERVICE	RECEIVE FIFO SERVICE SELECT • 000=NONE • 001=DMA • 010=INTERRUPT • 011=RESERVED • 1XX=RESERVED
20:19 (706)	READ/WRITE	RxTHRESH-LEVEL	RECEIVE FIFO SERVICE THRESHOLD • 00=4 BYTES • 01=8 BYTES • 10=16 BYTES • 11=32 BYTES
18 (708)	READ/WRITE	RxDFC ENABLE	DIRECT FLOW CONTROL ENABLE • 0=DISABLED • 1=ENABLED
17 (710)	READ/WRITE	RxMFC ENABLE	MESSAGE FLOW CONTROL ENABLE • 0=DISABLED • 1=ENABLED
16 (712)	READ/WRITE	RxENABLE	RECEIVE FIFO CHANNEL ENABLE • 0=CHANNEL DISABLED • 1=CHANNEL ENABLED
15:11	READ/WRITE	RESERVED	RESERVED
10:8	READ/WRITE	TxBLOCK	TRANSMIT BLOCK SIZE • 000=4 BYTES • 001=8 BYTES • 010=16 BYTES • 011=32 BYTES • 1XX=RESERVED
7:5 (704)	READ/WRITE	TxSERVICE	TRANSMIT FIFO SERVICE SELECT • 000=NONE • 001=DMA • 010=INTERRUPT • 011=RESERVED • 1XX=RESERVED
4:3 (706)	READ/WRITE	TxTHRESH-LEVEL	TRANSMIT FIFO SERVICE THRESHOLD • 00=4 BYTES • 01=8 BYTES • 10=16 BYTES • 11=32 BYTES
2 (708)	READ/WRITE	TxDFCENABLE	DIRECT FLOW CONTROL ENABLE • 0=DISABLED • 1=ENABLED
1 (710)	READ/WRITE	TxMFCENABLE	MESSAGE FLOW CONTROL ENABLE • 0=DISABLED • 1=ENABLED
0 (712)	READ/WRITE	TxENABLE	TRANSMIT FIFO CHANNEL ENABLE • 0=CHANNEL DISABLED • 1=CHANNEL ENABLED

Fig.7

512

INTERFACE INTERUPT IDENTIFICATION REGISTER			
BITS	ACCESS	NAME	DESCRIPTION
31:24	N/A	RESERVED	RESERVED
23:17	READ/WRITE 1 TO CLEAR	TX_INTx	TRANSMIT FIFO INTERRUPT FOR CHANNEL x
16	N/A	RESERVED	RESERVED
15:9	READ/WRITE 1 TO CLEAR	EOC_INTx	EOC INTERRUPT FOR CHANNEL x
8	N/A	RESERVED	RESERVED
7:1	READ/WRITE 1 TO CLEAR	RX_INTx	RECEIVE FIFO INTERRUPT FOR CHANNEL x
0	READ/WRITE 1 TO CLEAR	VGPIO_INT	VGPIO INTERRUPT – SEE BBVGED REGISTER FOR WHICH VGPIO PIN

Fig.8

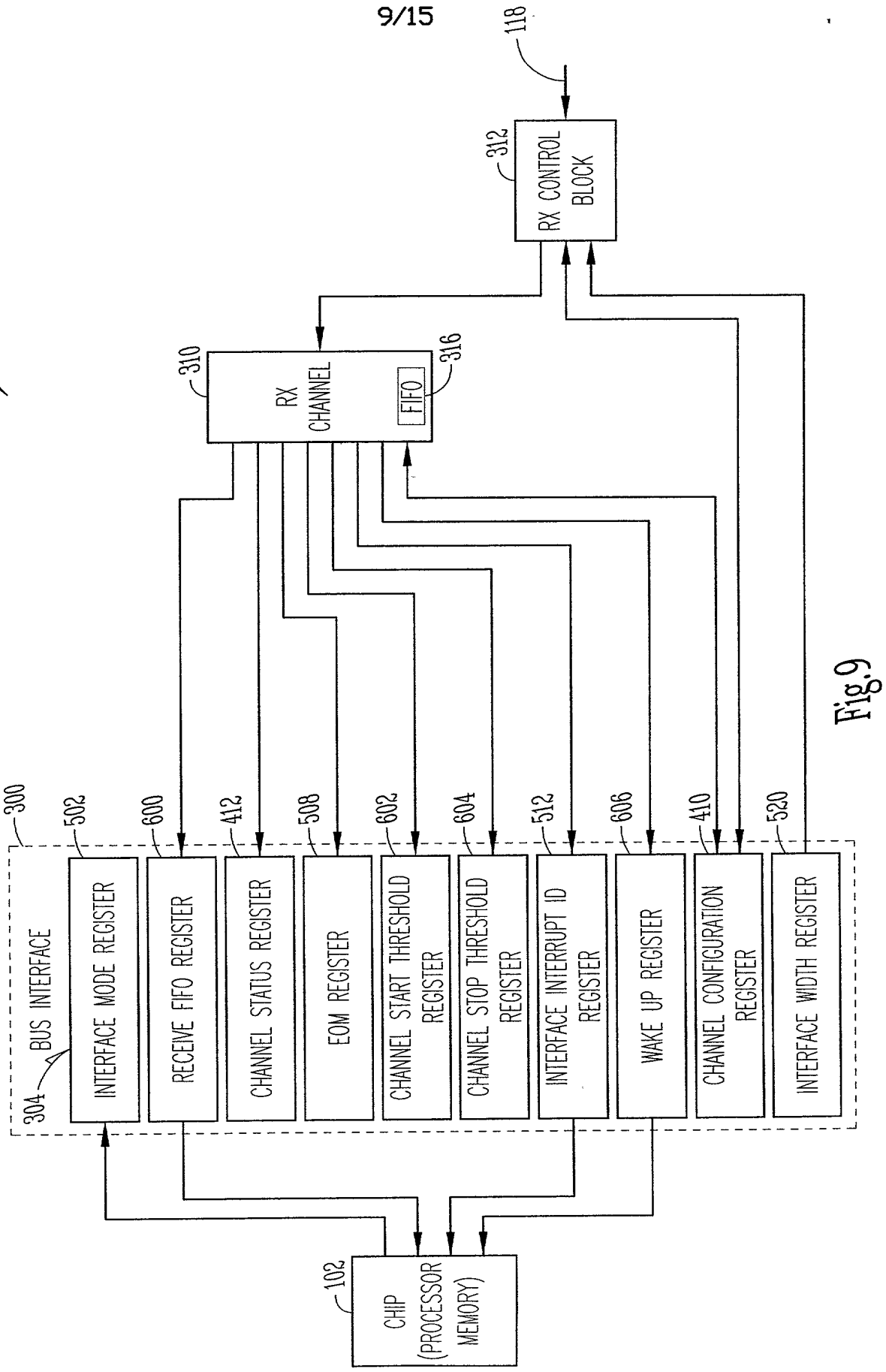
118
312
RX CONTROL BLOCK
112
310
RX CHANNEL
316
FIFO
300
BUS INTERFACE
304
502
INTERFACE MODE REGISTER
600
RECEIVE FIFO REGISTER
412
CHANNEL STATUS REGISTER
508
EOM REGISTER
602
CHANNEL START THRESHOLD REGISTER
604
CHANNEL STOP THRESHOLD REGISTER
512
INTERFACE INTERRUPT ID REGISTER
606
WAKE UP REGISTER
410
CHANNEL CONFIGURATION REGISTER
520
INTERFACE WIDTH REGISTER
102
CHIP (PROCESSOR MEMORY)

Fig.9

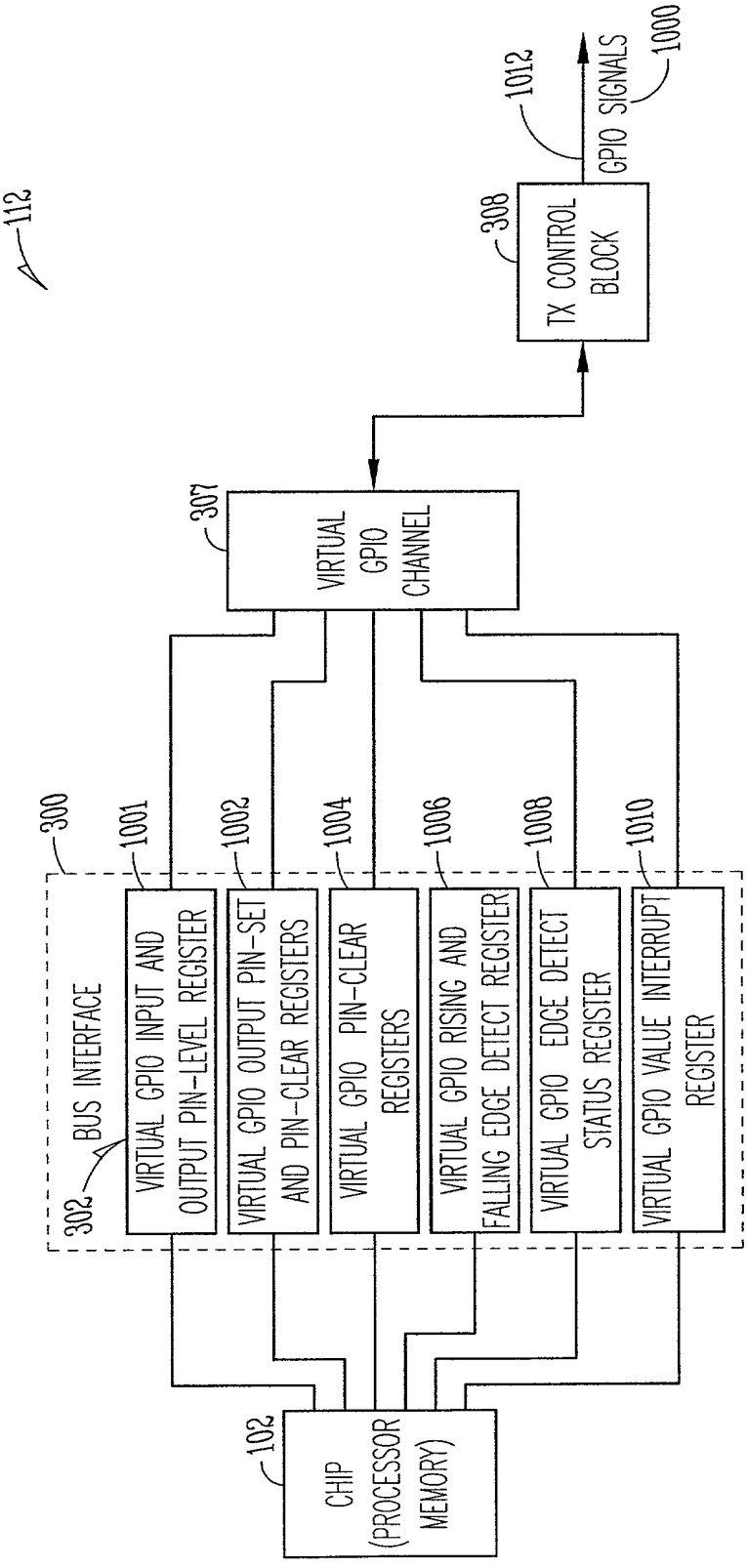
112
1000
GPIO SIGNALS
1012
308
TX CONTROL BLOCK
307
VIRTUAL GPIO CHANNEL
300
BUS INTERFACE
302
1001
VIRTUAL GPIO INPUT AND OUTPUT PIN-LEVEL REGISTER
1002
VIRTUAL GPIO OUTPUT PIN-SET AND PIN-CLEAR REGISTERS
1004
VIRTUAL GPIO PIN-CLEAR REGISTERS
1006
VIRTUAL GPIO RISING AND FALLING EDGE DETECT REGISTER
1008
VIRTUAL GPIO EDGE DETECT STATUS REGISTER
1010
VIRTUAL GPIO VALUE INTERRUPT REGISTER
102
CHIP (PROCESSOR MEMORY)

Fig.10

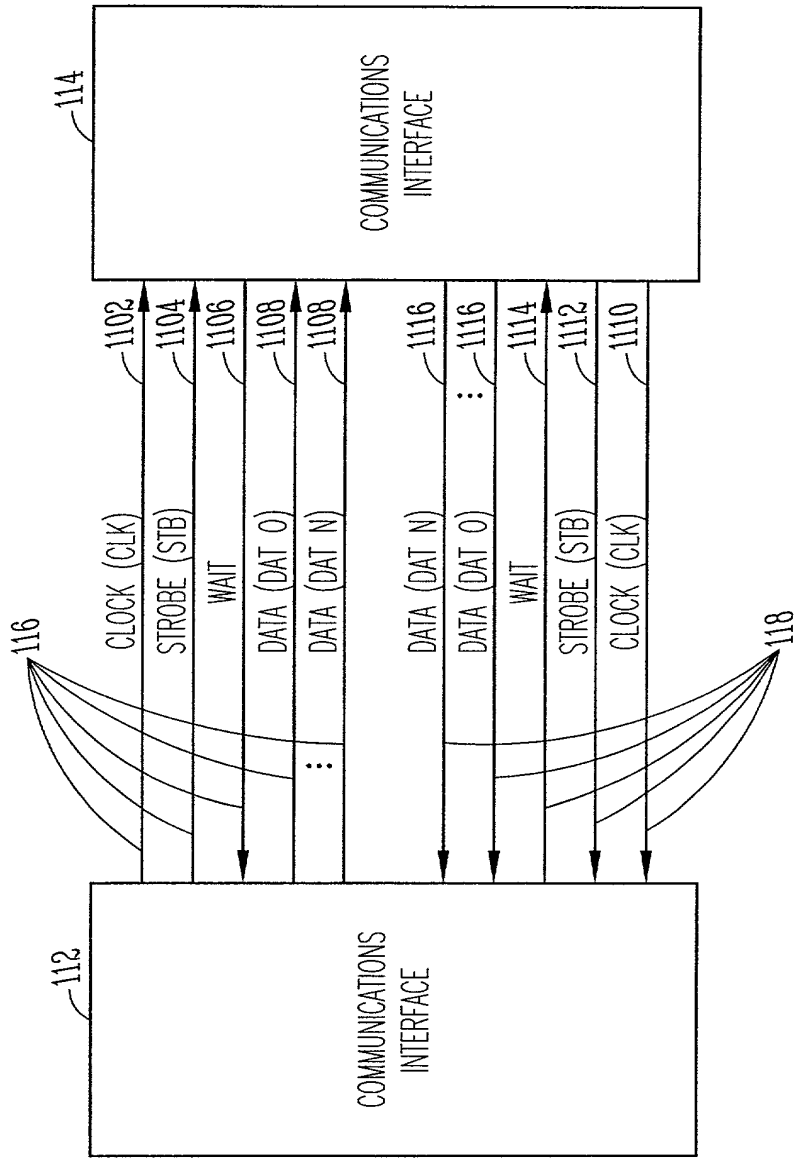
114
COMMUNICATIONS INTERFACE
1102
1104
1106
1108
1108
1116
1116
1114
1112
1110
CLOCK (CLK)
STROBE (STB)
WAIT
DATA (DAT 0)
DATA (DAT N)
DATA (DAT N)
DATA (DAT 0)
WAIT
STROBE (STB)
CLOCK (CLK)
116
118
112
COMMUNICATIONS INTERFACE

Fig.11

CHANNEL NUMBER	DESCRIPTION
0	NULL CHANNEL TO SIGNAL EOM
1	DATA CHANNEL 1
2	DATA CHANNEL 2
3	DATA CHANNEL 3
4	DATA CHANNEL 4
5	DATA CHANNEL 5
6	DATA CHANNEL 6
7	DATA CHANNEL 7
8	RESERVED
9	RESERVED
10 (A)	RESERVED
11 (B)	EMPTY CHANNEL
12 (C)	WAKE UP CHANNEL
13 (D)	VITTUAL GPIO CHANNEL
14 (E)	STOP MESSAGE CHANNEL
15 (F)	START MESSAGE CHANNEL

Fig.12

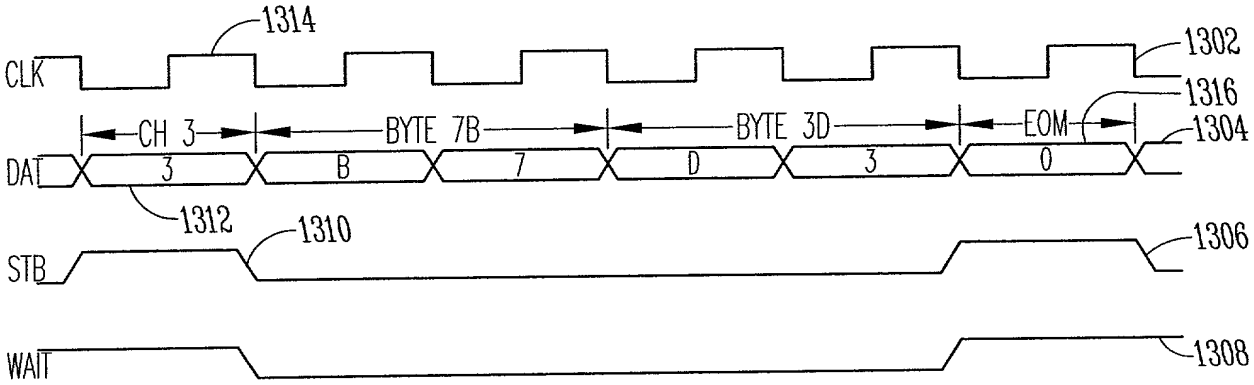
1314
CLK
1302
1316
CH 3
BYTE 7B
BYTE 3D
EOM
1304
DAT
3
B
7
D
3
0
1312
1310
1306
STB
WAIT
1308

Fig.13

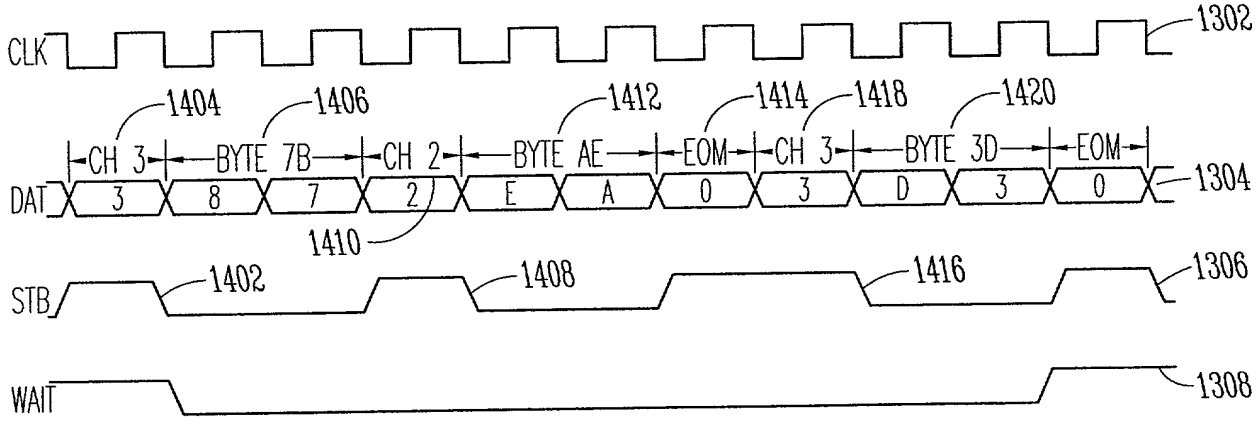
CLK
1302
1404
1406
1412
1414
1418
1420
CH 3
BYTE 7B
CH 2
BYTE AE
EOM
CH 3
BYTE 3D
EOM
DAT
3
8
7
2
E
A
0
3
D
3
0
1304
1410
1402
1408
1416
STB
1306
WAIT
1308

Fig.14

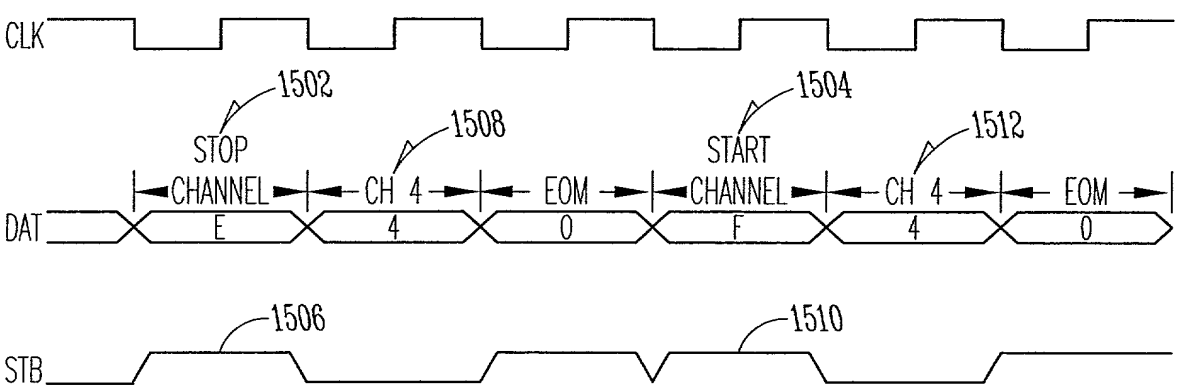
CLK
1502
1504
STOP
1508
START
1512
CHANNEL
CH 4
EOM
CHANNEL
CH 4
EOM
DAT
E
4
0
F
4
0
1506
1510
STB

Fig.15

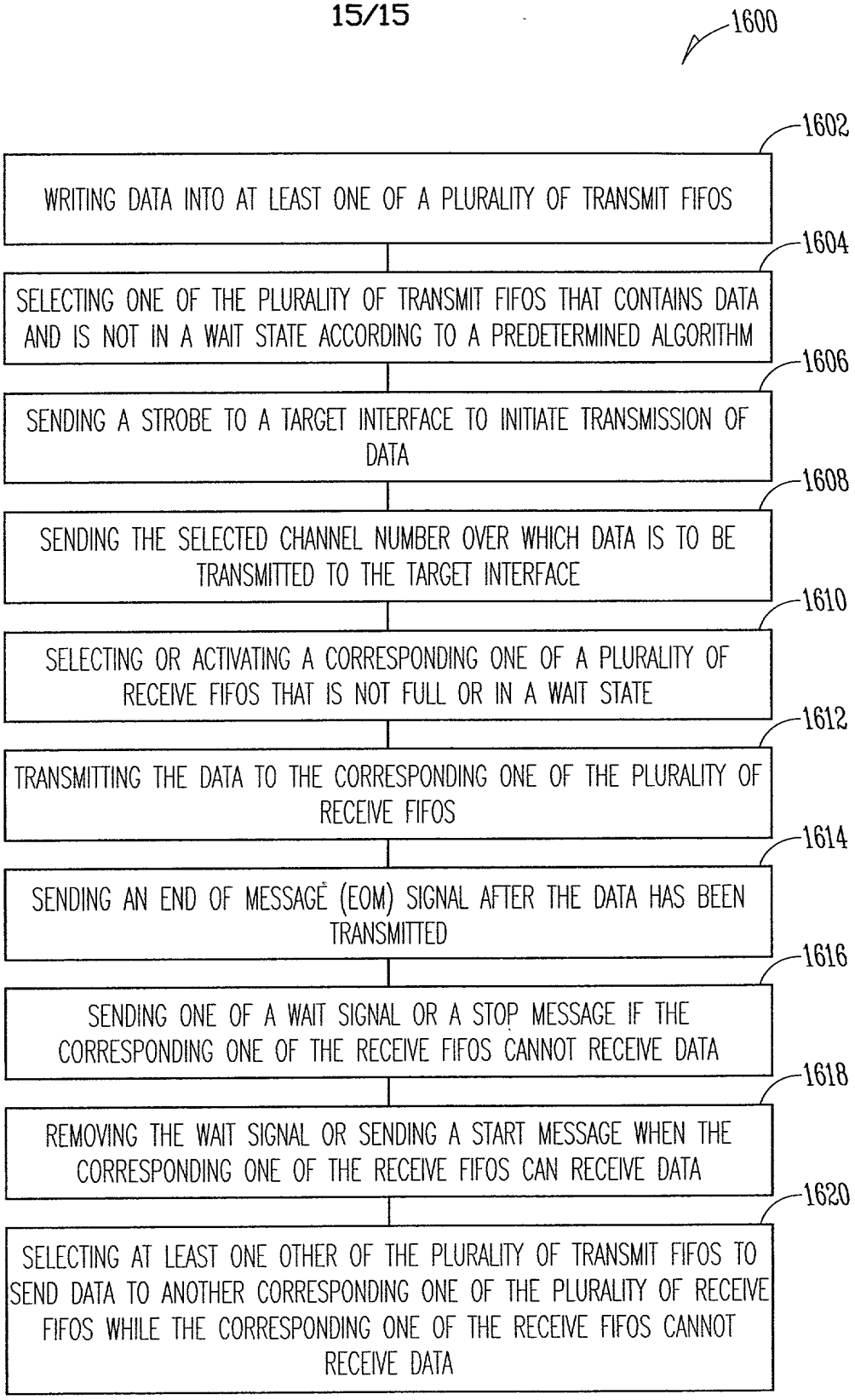
1600
1602
WRITING DATA INTO AT LEAST ONE OF A PLURALITY OF TRANSMIT FIFOS
1604
SELECTING ONE OF THE PLURALITY OF TRANSMIT FIFOS THAT CONTAINS DATA AND IS NOT IN A WAIT STATE ACCORDING TO A PREDETERMINED ALGORITHM
1606
SENDING A STROBE TO A TARGET INTERFACE TO INITIATE TRANSMISSION OF DATA
1608
SENDING THE SELECTED CHANNEL NUMBER OVER WHICH DATA IS TO BE TRANSMITTED TO THE TARGET INTERFACE
1610
SELECTING OR ACTIVATING A CORRESPONDING ONE OF A PLURALITY OF RECEIVE FIFOS THAT IS NOT FULL OR IN A WAIT STATE
1612
TRANSMITTING THE DATA TO THE CORRESPONDING ONE OF THE PLURALITY OF RECEIVE FIFOS
1614
SENDING AN END OF MESSAGE (EOM) SIGNAL AFTER THE DATA HAS BEEN TRANSMITTED
1616
SENDING ONE OF A WAIT SIGNAL OR A STOP MESSAGE IF THE CORRESPONDING ONE OF THE RECEIVE FIFOS CANNOT RECEIVE DATA
1618
REMOVING THE WAIT SIGNAL OR SENDING A START MESSAGE WHEN THE CORRESPONDING ONE OF THE RECEIVE FIFOS CAN RECEIVE DATA
1620
SELECTING AT LEAST ONE OTHER OF THE PLURALITY OF TRANSMIT FIFOS TO SEND DATA TO ANOTHER CORRESPONDING ONE OF THE PLURALITY OF RECEIVE FIFOS WHILE THE CORRESPONDING ONE OF THE RECEIVE FIFOS CANNOT RECEIVE DATA

Fig.16